REMARKS

This responds to the Office Action mailed on August 26, 2008.

No claims are amended, canceled, or added; as a result, claims 1-25 remain pending in this application.

§102 Rejection of the Claims

Claims 1-25 were rejected under 35 USC § 102(b) as being anticipated by Kennedy (U.S. 5,450,576; hereinafter "Kennedy"). Applicant respectfully traverses the rejection of claims 1-25 because Kennedy fails to teach or suggest all the elements of the claims.

For example, independent claims 1, 5, 8, 12, 16, and 21 include performing memory initialization commands at the level of a memory module. Applicant reiterates, and incorporates by this reference, the previous arguments of the last three Office Action responses as they are equally applicable here. In particular, Applicant respectfully submits that the claimed invention provides solutions where memory initialization and testing is performed in parallel at the memory module level rather than at the CPU or memory controller level. Kennedy is an example where memory initialization is performed at the CPU level.

Kennedy does include a memory module 130 with an associated ISTC (Initialize Self-Test Code) memory 129. However, as described in Kennedy, the ISTC memory 129 only includes code stored for easy access by a processor during initialization. Cole 5, line 51 – col. 6, line 24. Further, review of the "Distributed Initialize Function" portion of Kennedy reveals that the goal of the ISTC memories are to provide easier access to initialization code by CPUs for various components of a system during initialization. Col. 7, line 4 – col. 9, line 68. In particular, Kennedy provides that "[o]nce the ISTC is assembled in memory, it is executed from memory by the corresponding CPU, or executed by the boot CPU if the ISTC corresponds to a memory module or I/O circuit board." This highlights that Kennedy performs the memory initialization by execution in a boot processor and not by the memory modules as claimed.

The Office Action on pages 3 and 4 asserts that the memories 123 and 129 contain configuration information and ISTC for CPU1 120 and CPU2 132, respectively. Review of col.

5, lines 15-50 reveals that the ISTC for CPU1 120 and CPU2 132 is initialization code for the respective processors and not memories as claimed.

Applicant refers the Examiner's attention to FIG. 1 of the present application which illustrates how the processor 102 is distinct from the memory controller 104. Further, the memory modules 112, 114, 116 are distinct from the memory controller 104. Applicant's specification provides description as to the details of a processor in the paragraph beginning on line 17 of page 4. Description of the memory controller is found in the paragraph beginning at line 28 of page 4 and the following paragraphs. Description of the memory modules is found in the paragraph beginning at line 22 of page 5 and the following paragraphs. These descriptive portions of the specification, among others, provide background and definitions for the elements of the claims and highlight how the memory initialization and testing is performed by memory modules in response to commands originating with a processor and may be communicated via a memory controller. Further, FIG. 2, and its description beginning at line 7 of page 8, illustrates how a memory module includes memory storage units.

Applicant respectfully submits that this highlights what a memory module, as included in the claims, is and is not. A memory module is not a memory controller 36 and is not a CPU 30 as in Kennedy. Further, a memory module may include memory storage units, but is more than a portion of system memory. A memory module, as claimed, provides an additional level of memory management and allows for finer grained parallel memory initialization and testing. This level of memory management allows for performance of memory initialization and memory test procedures within the memory module. This is in specific contrast to performance of the ISTC by the CPUs of Kennedy.

Applicant respectfully submits that independent claims 1, 5, 8, 12, 16, and 21 are patentable over Kennedy at least because Kennedy fails to teach or suggest the following portions of the claims:

> 1. performing a first memory access procedure, in response to. . . a command bus from a memory controller, wherein the first memory access procedure causes *a memory module to perform* . . . a memory initialization procedure and a memory test procedure.
>
> 5. … performing, within a memory module, an initialization procedure,….

8. … performing a testing procedure, in response to the test command, during which the memory module tests one or more memory storage units….

12. … a first memory module performing a first memory access procedure, … the first memory access procedure is selected from a group of procedures that includes a memory initialization procedure and a memory test procedure; and

at least one additional memory module performing a second memory access procedure … wherein the first memory access procedure and the second memory access procedure include substantially similar process steps, and wherein at least a portion of the first memory access procedure is performed in parallel with at least a portion of the second memory access procedure.

16. … a first memory module performing a first initialization procedure of first memory locations associated with the first memory module …;

at least one additional memory module performing at least one additional initialization procedure of second memory locations associated with the at least one additional memory module….

21. … selected ones of the multiple memory modules performing an initialization procedure in parallel….

Thus, for at least these reasons, Applicant respectfully submits that Kennedy fails to teach or suggest all the limitations of the claims 1-25, and in particular the memory modules that perform initialization included in each of the independent claims 1, 5, 8, 12, 16, and 21.

Applicant respectfully requests withdrawal of the 35 U.S.C. § 102(b) rejections and allowance of claims 1-25.

CONCLUSION

Applicant respectfully submits that claims 1-25 are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6938 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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